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ELECTROSTATIC DISCHARGE (ESD) PROTECTION MOS DEVICE AND ESD CIRCUITRY THEREOF

Abstract

An NMOS device having protection against electrostatic discharge. The NMOS device includes a P-substrate, a P-epitaxial layer overlying the P-substrate, a P-well in the P-epitaxial layer, an N-well in the P-epitaxial layer and encompassing the P-well, an N-Buried Layer (NBL) underneath the P-well and bordering the N-well. The P-well is fully isolated by the N-well and the NBL. The NMOS device further includes a first isolation structure consisting of a gate-insulating layer connected with a field oxide layer, which is formed on the P-epitaxial layer. A gate overlies the first isolation structure. A second isolation structure laterally spaced apart from the first isolation structure is approximately situated on the N-well. An N^+ source doping region, which functions as a source of the NMOS device, is disposed in the P-well. An N^+ drain doping region, which functions as a drain of the NMOS device, is disposed in the N-well.